REMARKS/ARGUMENTS

Applicants thank the Examiner for the careful consideration given the present application, and respectfully request favorable reconsideration of the application in view of the comments set forth below.

Applicants note, with appreciation, the identification of claim 34 as being allowable if rewritten in independent form, including the limitations from all underlying base claims from which it depends. Claim 34, however, has been amended to remove redundant limitations already included in claim 1, and to correct other informalities.

Claim Rejections - 35 USC §112

Claims 1, 5-9, 13, 14 and 32-38 are rejected under 35 U.S.C. §112, ¶2, as being indefinite for reciting features separated by a slash. Claim 1 has been amended to delete the "/" character and the reference to the "rectified current". Accordingly, Applicants respectfully submit that claim 1 is fully compliant with 35 U.S.C. §112.

Claim Rejections - 35 USC §103

Claims 1, 6 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bessyo (US 6,362,463) in view of Suenaga (JP 2004-030981) (hereinafter "Suenaga") and Kamimura (JP 62-66595 (herenafter "Kamimura"). Applicants respectfully submit that the combination of Bessyo, Suenaga and Kamimura fails to teach, suggest or otherwise render obvious every claimed feature as required to maintain the present rejection.

Specifically, amended claim 1 recites a frequency-modulated signal generation circuit that outputs to the dead time generation circuit a frequency-modulated signal obtained by controlling an amplitude of a rectified voltage signal output from the DC power supply based on the error signal. By way of example, the embodiment illustrated in FIG. 5 of the present application includes a frequency-modulated signal generation circuit 22 that generates a frequency-modulated signal based on the signals from the error signal generation circuit 21 and an AC full-wave signal. *See also*, pg. 23, line 16 – pg. 17, line 6. The frequency-modulated

signal is then transmitted to the dead time generation circuit 24, which generates a dead time control signal that is subsequently used to control the timing of switching the semiconductor switching devices 6, 7. Thus, the output from the frequency-modulated signal generation circuit is required to be output to the dead time generation circuit so the control signal for turning off the semiconductor switching devices can be transmitted to those semiconductor switching devices.

In contrast, Bessyo is correctly acknowledged in the Office action as lacking the claimed frequency-modulated signal generation circuit, which is also absent from the teachings of Kamimura. And the portions of Suenaga cited as teaching the claimed frequency-modulated signal generation circuit, actually describe a pulse-width modulation ("PWM") circuit 82 that outputs the actual control signal directly to the switching device 39 therein. Suenaga, like Bessyo and Kamimura, fails to teach, suggest or otherwise render obvious a frequency-modulated signal generation circuit that outputs a frequency modulated signal obtained by controlling a signal from the DC power supply to a dead time generation circuit as claimed in claim 1. The switching device 39 in Suenaga can not be interpreted as the claimed dead time generation circuit because the dead time generation is required to generate the dead time control signal to be used for controlling the claimed switching devices. Interpreting the switching device 39 in Suenaga as the dead time generation circuit would amount to a switching device that generated a dead time control signal to control its own operation, which is an unreasonable interpretation.

For at least the above reasons, the combination of Bessyo, Suenaga and Kamimura fails to teach every limitation found in claim 1 as required to maintain a rejection of that claim under 35 U.S.C. §103(a).

The remaining claims in the present application are allowable for the limitations therein and for the limitations of the claims from which they depend.

In consideration of the foregoing analysis, it is respectfully submitted that the present application is in a condition for allowance and notice to that effect is hereby requested. If it is determined that the application is not in a condition for allowance, the examiner is invited to initiate a telephone interview with the undersigned attorney to expedite prosecution of the present application.

If there are any additional fees resulting from this communication, please charge same to our Deposit Account No. 16-0820, our Order No.: 41339.

Respectfully submitted,
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